

Cont'd C1
already written, so that data can be written in only said memory cells to which data have not been properly written;

a plurality of data detecting circuits each connected to a predetermined number of said data storing circuits, each for detecting data stored in each of said data storing circuits and outputting the detected data when data are read for write verify; and

a write end detecting circuit for receiving output signals outputted by said data detecting circuits and for outputting a write completion signal when all the output signals indicate that data are written properly in said memory cells in which data are to be written.

REMARKS

Claim 99 being added by this Amendment is an exact copy of claim 1 of the U.S. patent no. 5,793,696 - Tanaka et al., granted August 11, 1998. It is being added to this application since it pertains to non-volatile memory program inhibit, the same subject matter of the claims pending in the present application that were copied from U.S. patent no. 5,657,270 - Ohuchi et al. Both of the Tanaka et al. and Ohuchi et al. patents are assigned on their faces to Kabushiki Kaisha Toshiba of Japan.

The matter of whether to request an interference with the Tanaka et al. patent is currently being reviewed by the undersigned.

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Respectfully submitted,

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